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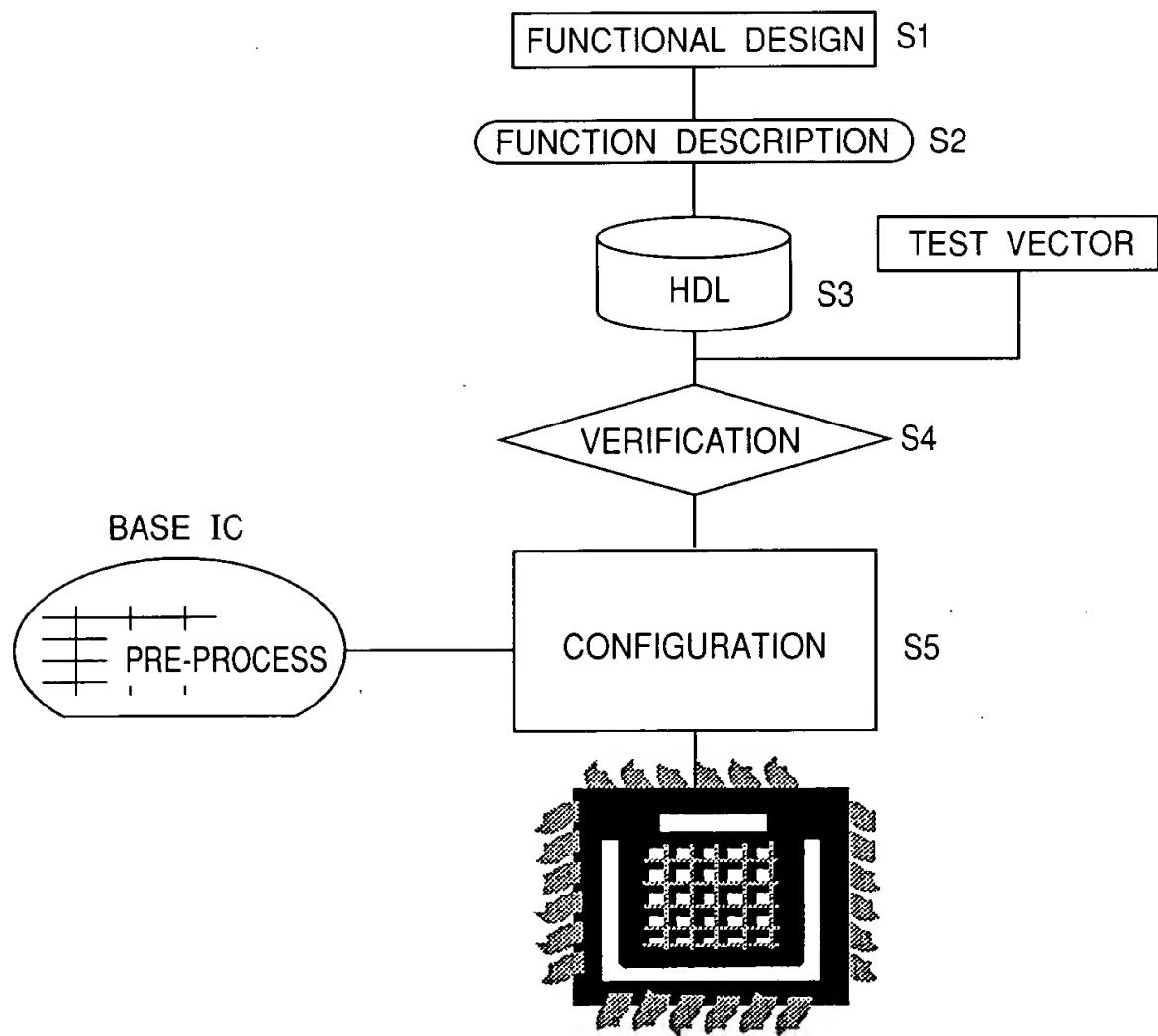
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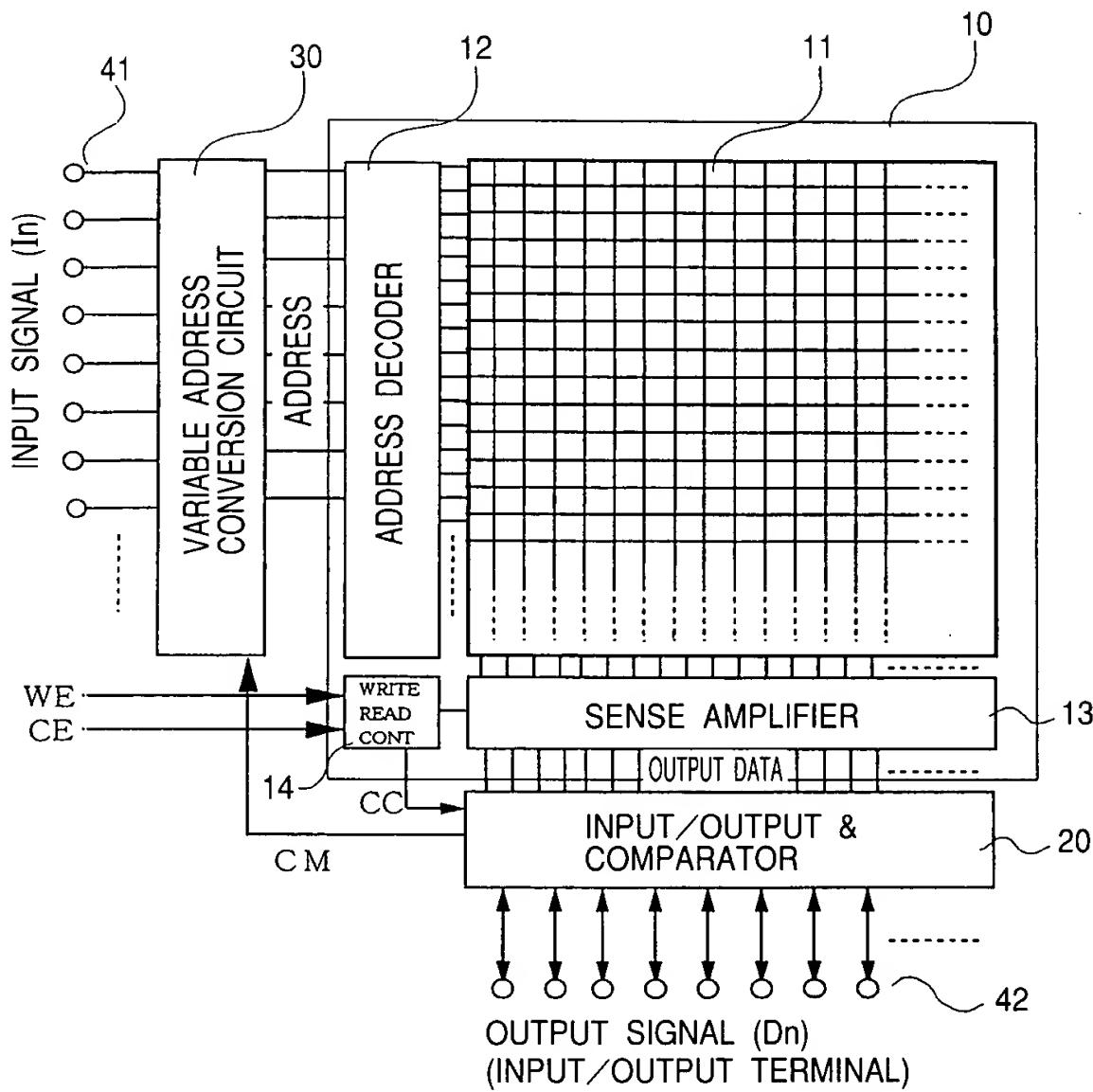
FIG. 1



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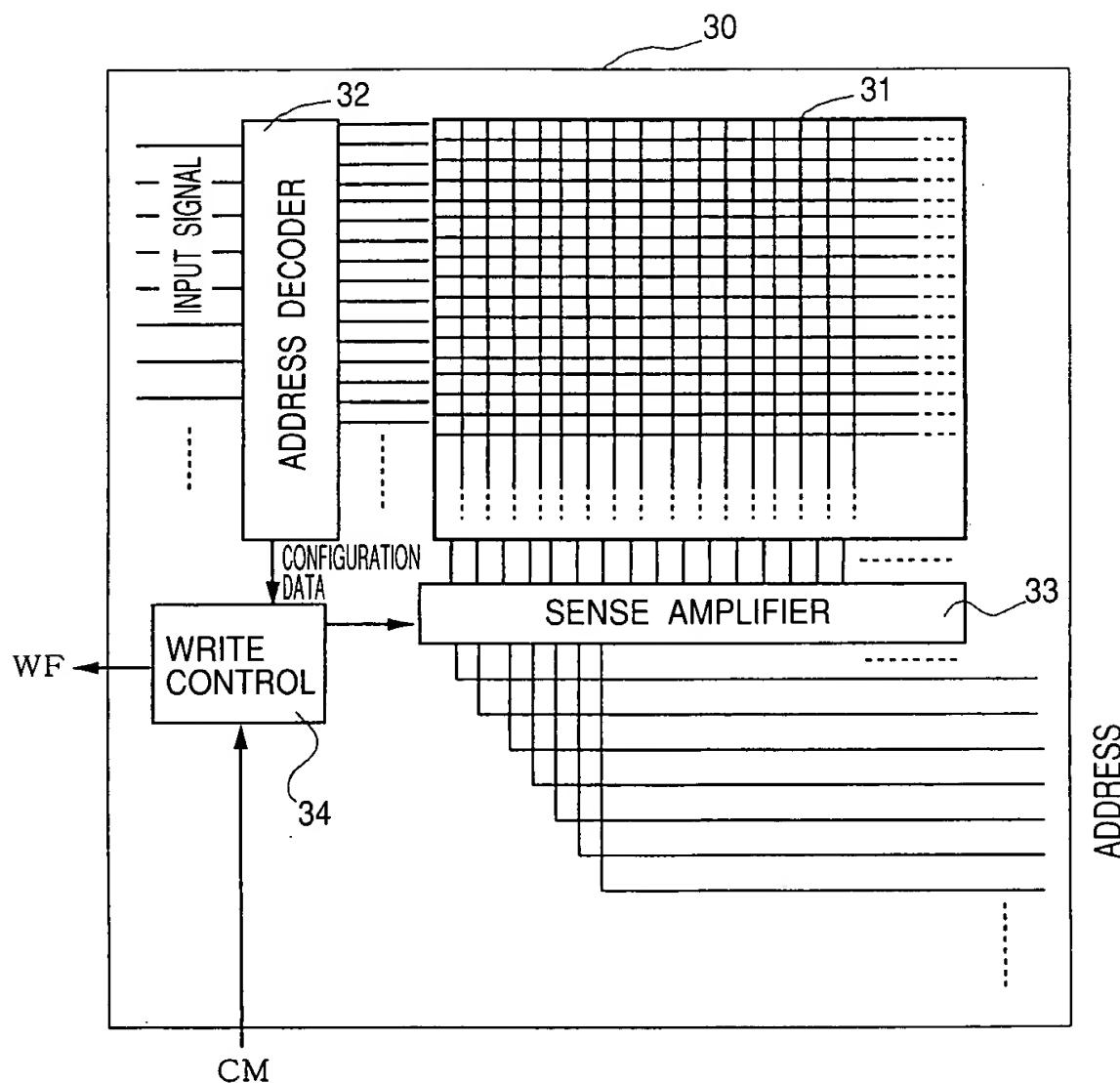
FIG. 2



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FIG. 3

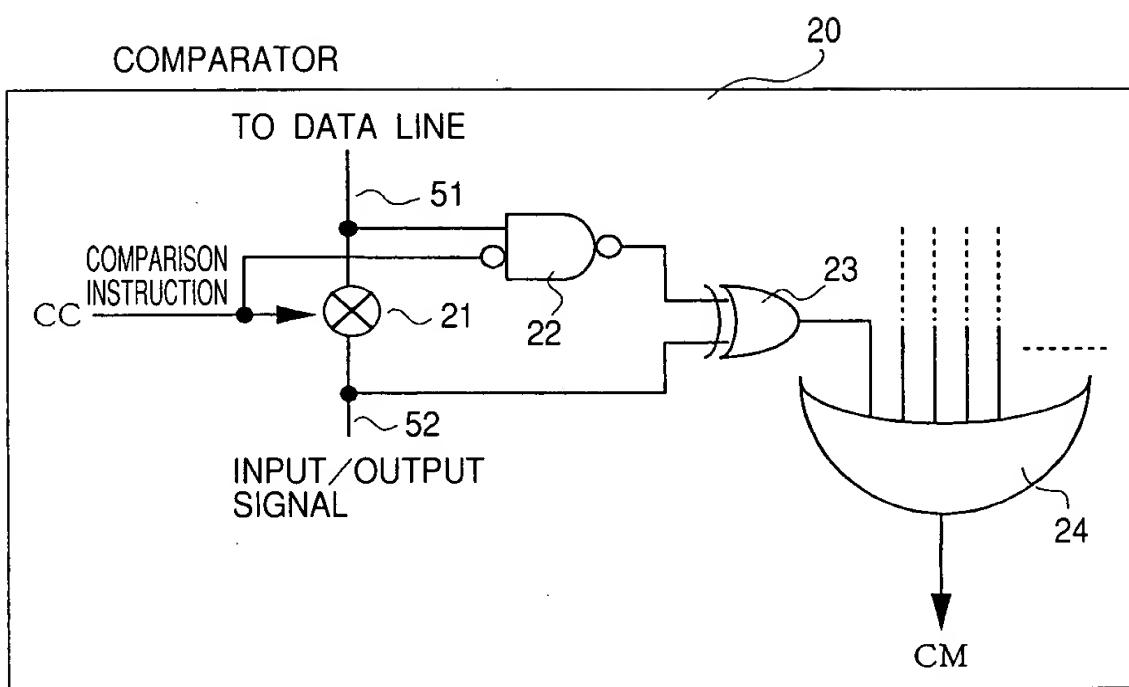


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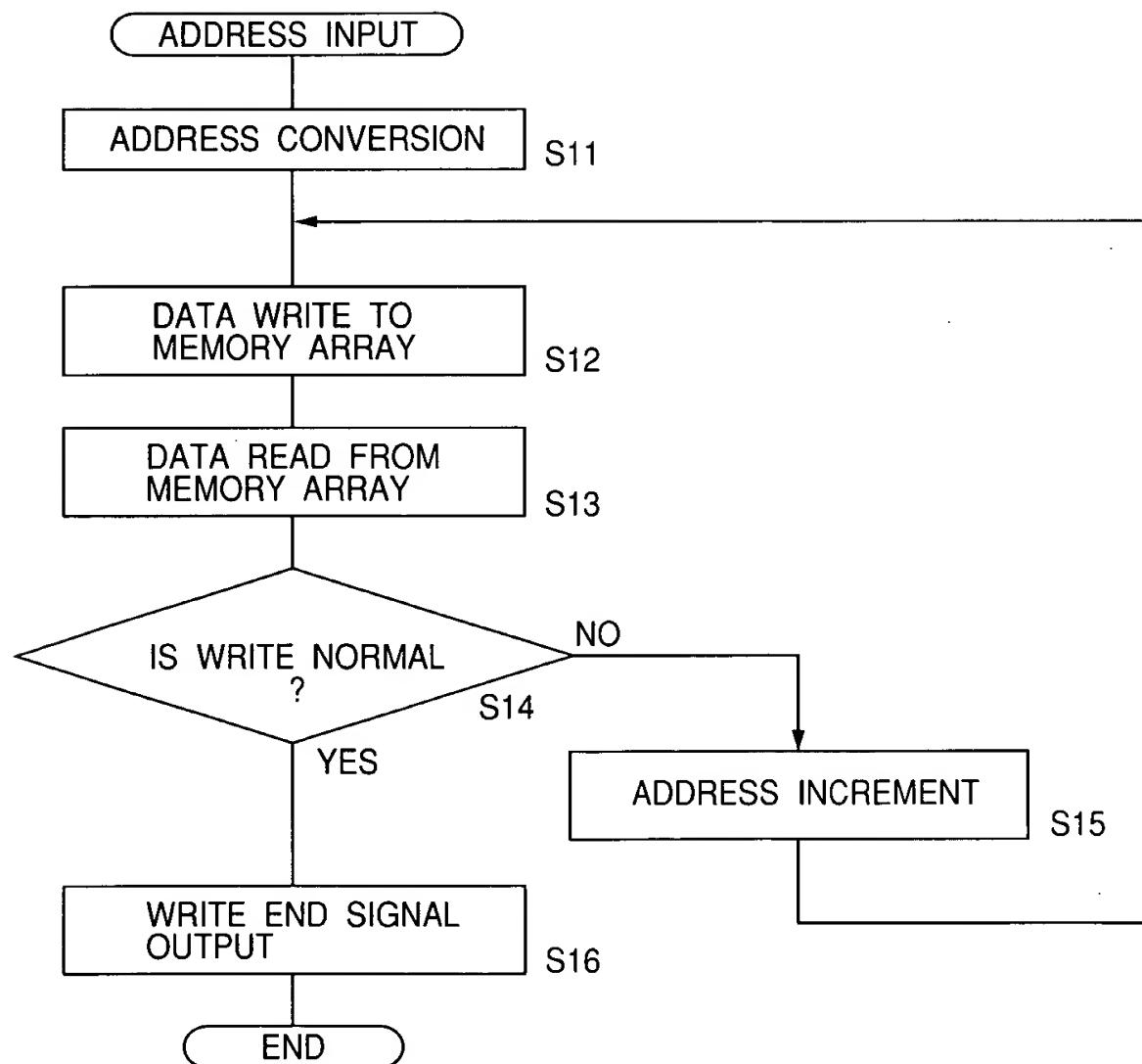
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FIG. 4



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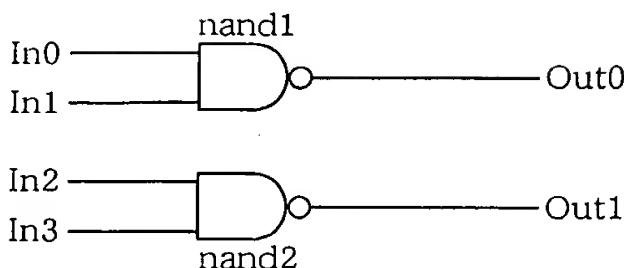
FIG. 5

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FIG. 6



HDL DESCRIPTIVE STATEMENT

//External Declaration

module nand1_gate(
 In0;
 In1;
 Out0
)

//Internal Declarations

input In0;
input In1;wire In0;
wire In1;
reg Out0;

always @ (In0 or In1) begin

```

//Block 1
case(In0, In1)
  2'b 00: Out0=1'b1;
  2'b 01: Out0=1'b1;
  2'b 10: Out0=1'b1;
  2'b 11: Out0=1'b0;
  default
  ;
endcase

```

end
endmododule // nand1_gate

//External Declaration

module nand2_gate(
 In2;
 In3;
 Out1);

//Internal Declarations

input In2;
input In3;wire In2;
wire In3;
reg Out1;

always @ (In2 or In3) begin

```

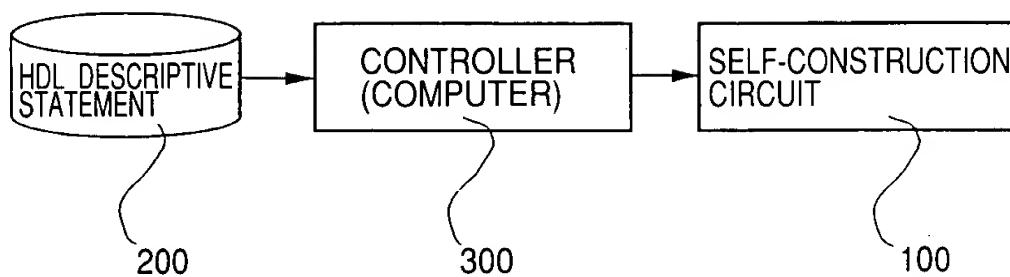
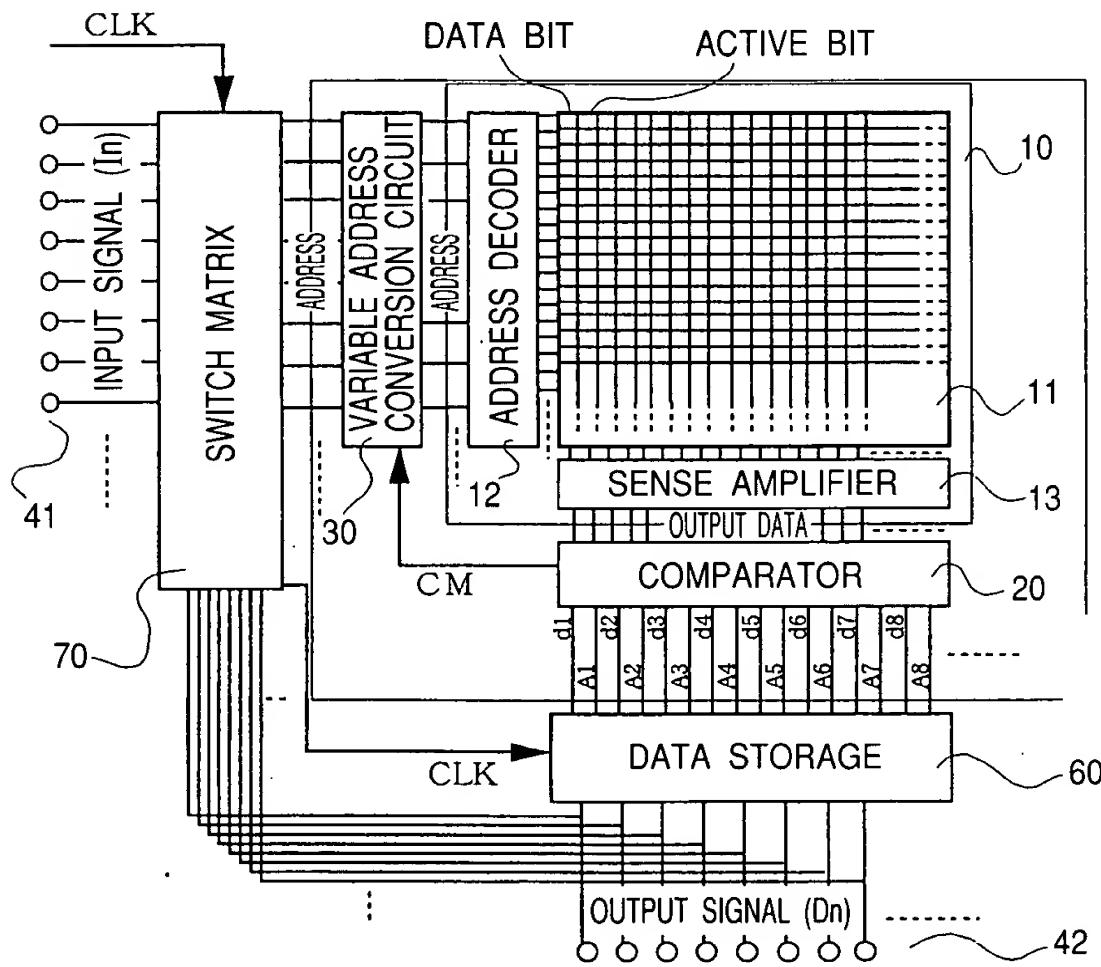
//Block 1
case(In2, In3)
  2'b 00: Out1=1'b1;
  2'b 01: Out1=1'b1;
  2'b 10: Out1=1'b1;
  2'b 11: Out1=1'b0;
  default
  ;
endcase

```

end
endmododule // nand1_gate2

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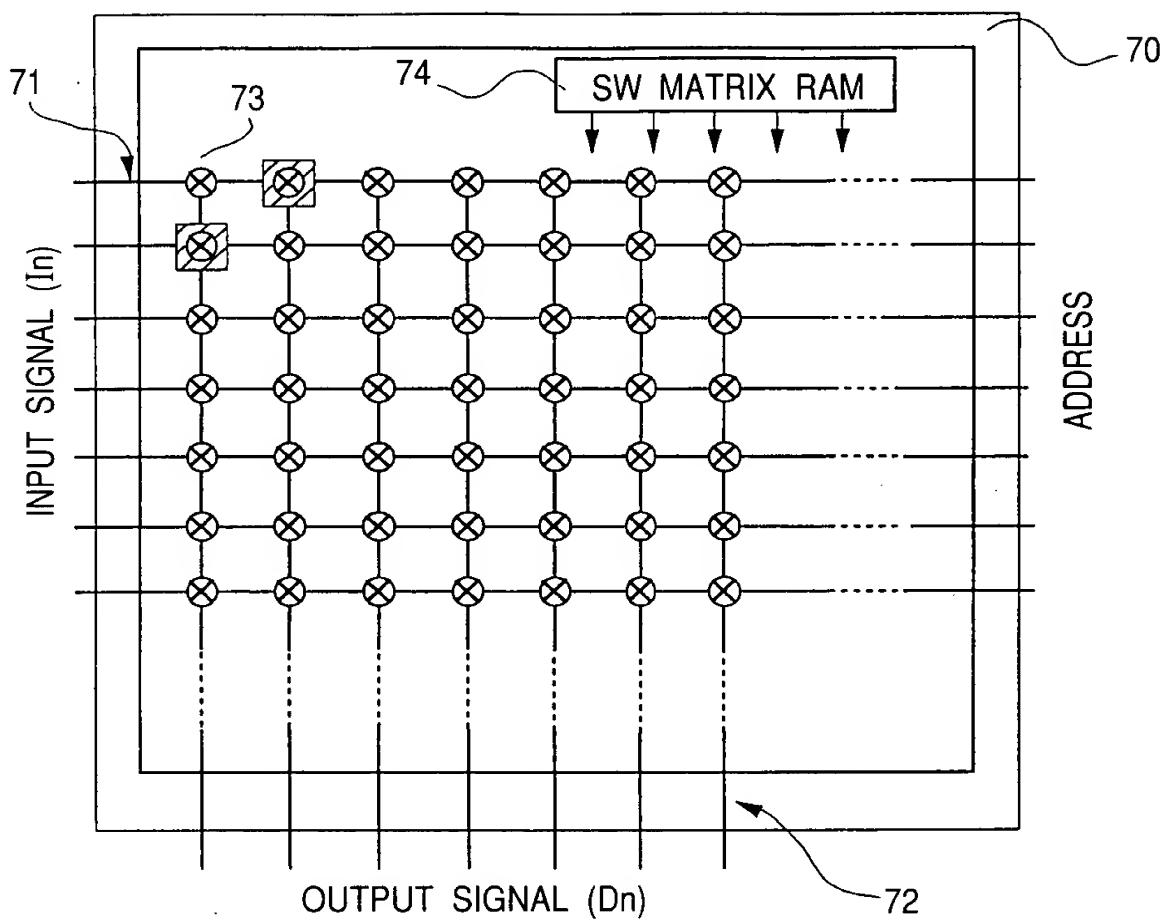
FIG. 7**FIG. 8**

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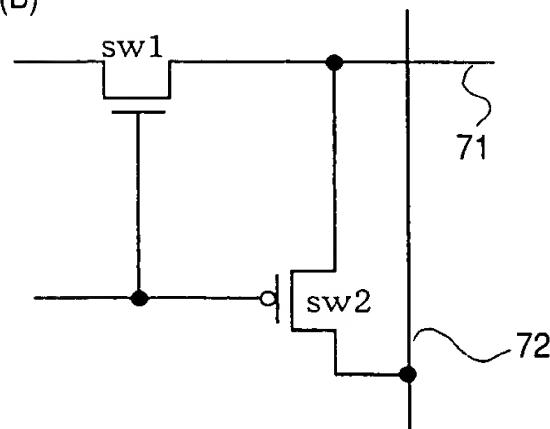
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FIG. 9

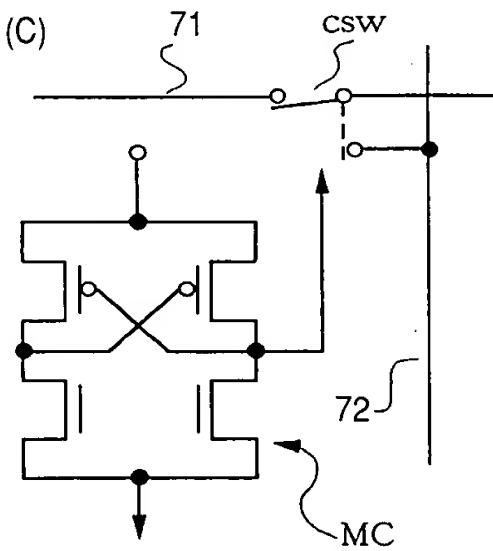
(A)



(B)



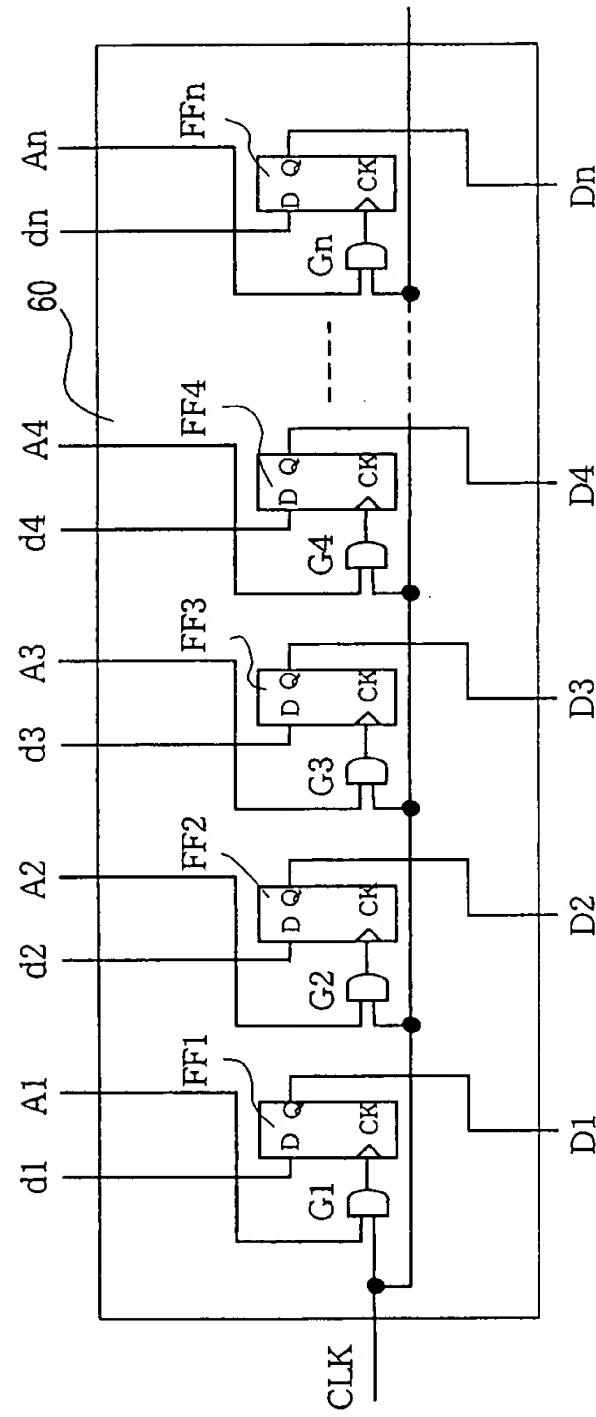
(C)



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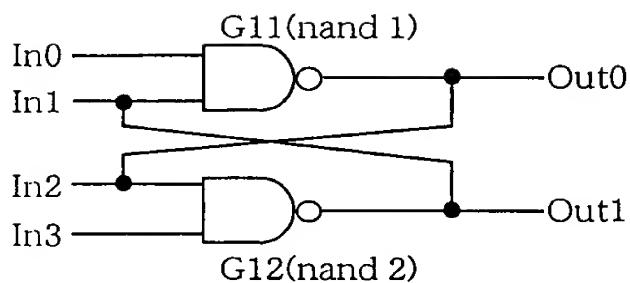
FIG. 10



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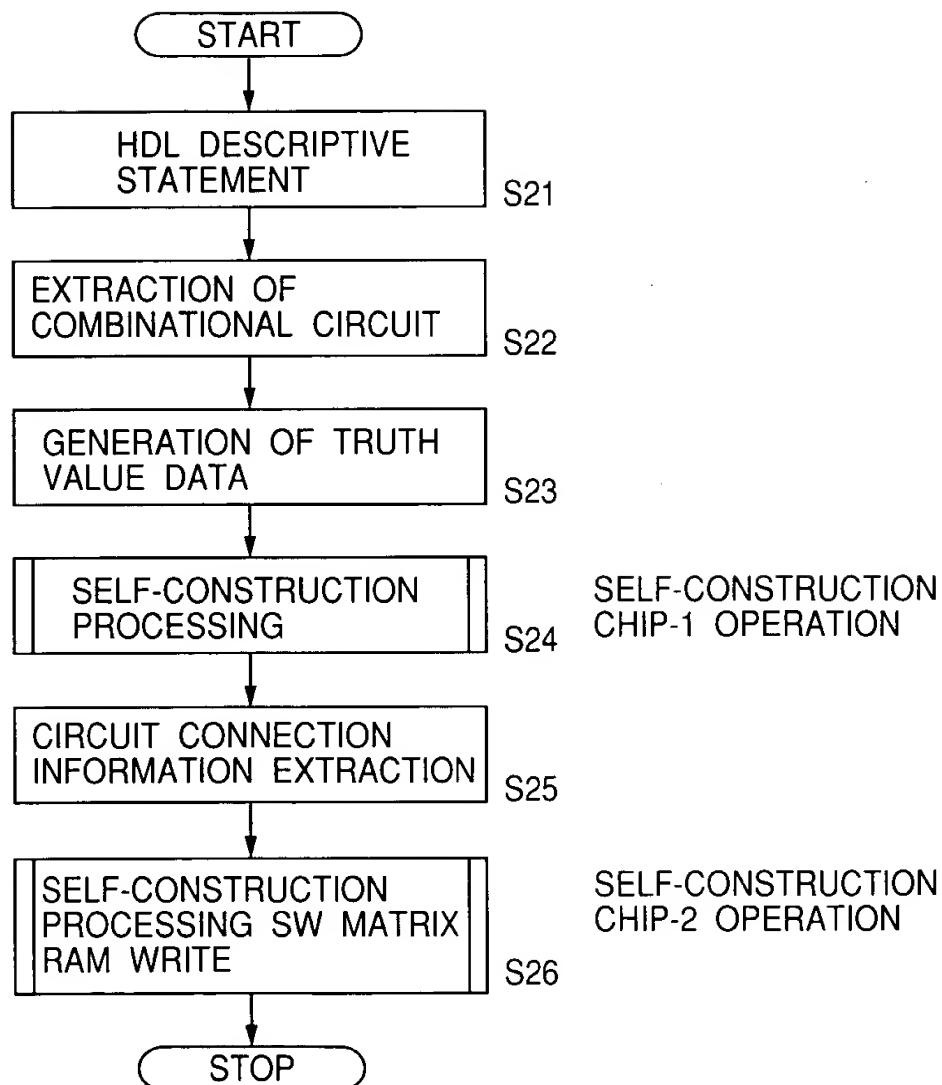
FIG. 11**HDL DESCRIPTIVE STATEMENT**

```

//External Declaration
module ff model(
  In0,
  In1,
  Out0,
  Out1
);
//Internal Declarations
input In0;
input In1;
output Out0;
output Out1;
wire In0;
wire In1;
reg Out0;
reg Out1;
//Local declarations
//Instances
nand1_gate(
  .In0(In0),
  .In1(Out1),
  .Out0(Out0),
);
nand2_gate(
  .In2(Out0),
  .In3(In3),
  .Out0(Out1)
);
endmodule // ff_model
  
```

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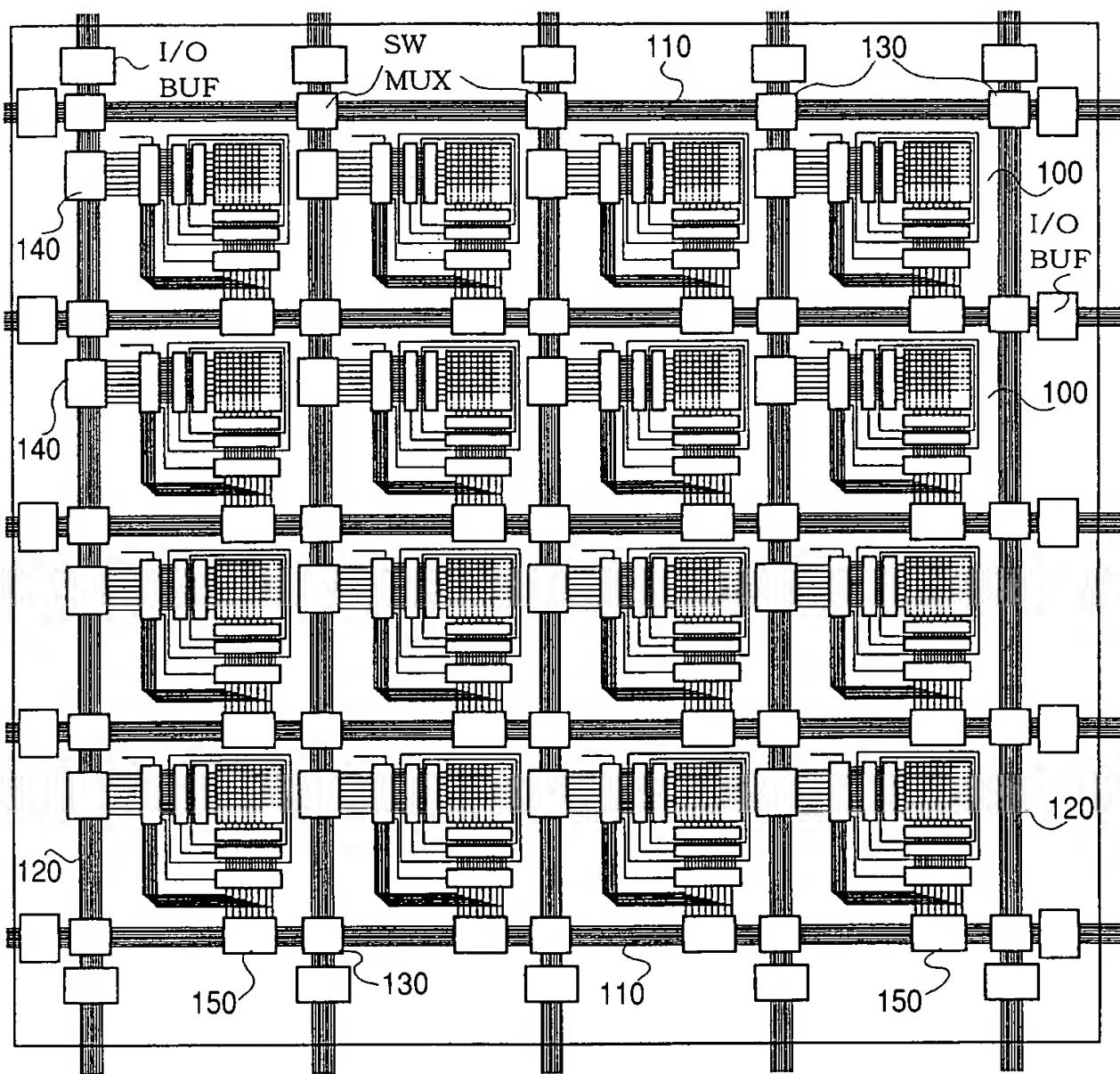
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FIG. 12

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FIG. 13

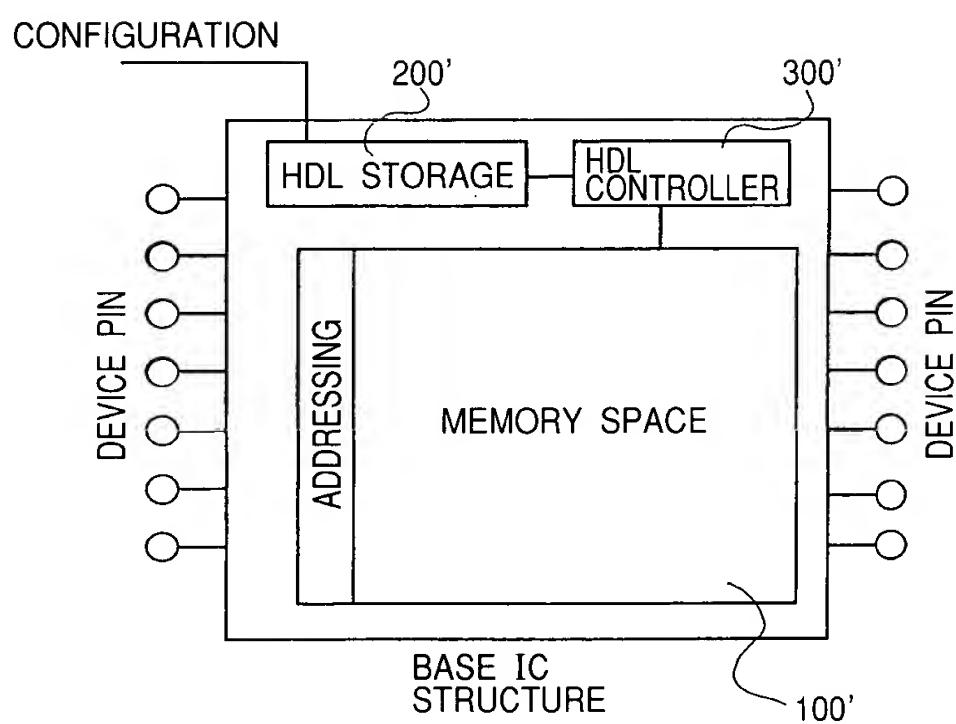


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FIG. 14



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FIG. 15

